LISTING OF CLAIMS IN THE CASE

Please amend Claims 1 and 11.

Please add Claims 12-92.

Claim 1. (Currently Amended) A method for controlling ~~the operating condition~~ power consumption of a computer processor on a chip comprising the steps of:

determining a maximum allowable power consumption level from ~~the~~ an operating condition of the processor,

determining a maximum frequency which provides power not greater than the allowable power consumption level,

determining a minimum voltage which allows operation at the maximum frequency determined, and

dynamically changing the ~~operating condition~~ power consumption of the processor by changing ~~one of the~~ frequency ~~frequencies generated by the clock generator~~ and ~~the~~ voltage, respectively, to the maximum frequency and the minimum voltage determined~~, wherein a plurality of clock frequencies are provided which can be individually selected concurrently~~.

Claim 2. (Currently Amended) A computing device comprising:

a power supply furnishing selectable output voltages,

a clock frequency source,

a central processor including:

a processing unit for providing values indicative of operating conditions of the central processor, and

a clock frequency generator receiving a clock frequency from the clock frequency source and providing ~~a~~ one of a plurality of selectable output clock frequencies to the processing unit; and

means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies

which are selected for optimum operation of a plurality of functional units of the computing device.

Claim 3. (Original) A computing device as claimed in Claim 2 in which the means for detecting the values indicative of operating conditions of the central processor comprises control software for determining an output clock frequency and voltage level for the central processor adapted to conserve power while maintaining an effective execution rate.

Claims 4-5 (Cancelled)

Claim 6. (Previously Amended) A method for controlling the power used by a computer comprising the steps of:

utilizing control software to measure the operating characteristics of a central processor of the computer,

determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted, and

changing the operating characteristics of the central processor to a level commensurate with the operations being conducted in which:

the step of determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted comprising utilizing the control software to determine desirable voltages and frequencies for the operation of the central processor based on the measured operating characteristics, and

the step of changing the operating characteristics of the central processor to a level commensurate with the operations being conducted comprises providing signals:

for controlling voltages furnished by a programmable power supply to the central processor,

for controlling frequencies furnished by the central processor to the central processor, and

providing signals for controlling frequencies furnished by the central processor to other functional units of the computer.

Claim 7. (Cancelled)

8. (Previously Amended) A computer comprising:

a power supply furnishing selectable output voltages,

a clock frequency source,

a bus,

system memory,

a central processor including:

a processing unit for providing values indicative of operating conditions of the central processor, and

a clock frequency generator receiving a clock frequency from the clock frequency source and providing a plurality of selectable output clock frequencies to the processing unit; and

means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device including system memory.

Claim 9. (Original) A computer as claimed in Claim 8 in which the means for detecting the values indicative of operating conditions of the central processor comprises control software for determining an output clock frequency and voltage level for the central processor adapted to conserve power while maintaining an effective execution rate.

Claim 10. (Previously Amended) A computing device as claimed in Claim 8 in which the means for detecting the values indicative of operating conditions of

the central processor causes the clock frequency generator to generate frequencies with are selected for optimum operation of system memory.

Claim 11. (Currently Amended) A computing device as claimed in Claim 8 in which the means for detecting the values indicative of operating conditions of the central processor causes the clock frequency generator to generate frequencies which are selected for optimum operation of ~~including~~ the bus.

Claim 12. (New) A method of controlling a computer processor, comprising:

monitoring operating conditions internal to said computer processor;

determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and

implementing the determined frequency and voltage.

Claim 13. (New) The method of Claim 12, wherein said implementing comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 14. (New) The method of Claim 13, wherein said implementing further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 15. (New) The method of Claim 12, wherein said implementing comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 16. (New) The method of Claim 12, wherein said implementing comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 17. (New) The method of Claim 13, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 18. (New) The method of Claim 13, wherein said implementing further comprises:

executing instructions in said computer processor after lowering frequency at which said computer processor is operated; and

then lowering voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 19. (New) The method of Claim 13, wherein said implementing further comprises:

lowering voltage at which said computer processor is operated; and

then executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 20. (New) A method of controlling a computer processor, comprising:

monitoring idle time of said computer processor;

determining a frequency and a voltage at which to operate said computer processor, based on said idle time; and

implementing the determined frequency and voltage.

Claim 21. (New) The method of Claim 20, wherein said implementing comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 22. (New) The method of Claim 21, wherein said implementing further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 23. (New) The method of Claim 20, wherein said implementing comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 24. (New) The method of Claim 20, wherein said monitoring idle time comprises monitoring internal data of said computer processor.

Claim 25. (New) The method of Claim 20, wherein said implementing comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 26. (New) The method of Claim 21, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 27. (New) The method of Claim 21, wherein said implementing further comprises:

executing instructions in said computer processor after lowering frequency at which said computer processor is operated; and

then lowering voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 28. (New) The method of Claim 21, wherein said implementing further comprises:

lowering voltage at which said computer processor is operated; and

then executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 29. (New) A method of controlling a computer processor, comprising:

monitoring a state of said computer processor;

determining a frequency and a voltage at which to operate said computer processor, based on said state; and

implementing the determined frequency and voltage.

Claim 30. (New) The method of Claim 29, wherein said state comprises a sleep state.

Claim 31. (New) The method of Claim 30, wherein said monitoring further comprises monitoring a halt state of said computer processor.

Claim 32. (New) The method of Claim 29, wherein said state comprises a halt state.

Claim 33. (New) The method of Claim 29, wherein said implementing comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 34. (New) The method of Claim 33, wherein said implementing further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 35. (New) The method of Claim 29, wherein said implementing comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 36. (New) The method of Claim 29, wherein said implementing comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 37. (New) The method of Claim 33, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 38. (New) The method of Claim 33, wherein said implementing further comprises:

executing instructions in said computer processor after lowering frequency at which said computer processor is operated; and

then lowering voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 39. (New) The method of Claim 33, wherein said implementing further comprises:

lowering voltage at which said computer processor is operated; and

then executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 40. (New) A method of controlling a computer processor, comprising:

a) monitoring operating temperature of said computer processor;

b) based on said operating temperature, determining that said computer processor can be operated at a higher frequency than a frequency at which said computer processor is currently operating without exceeding a threshold of said operating temperature; and

c) increasing a frequency at which said computer processor operates above said current frequency.

Claim 41. (New) The method of Claim 40, wherein said determining further comprises determining a time for which to operate said computer processor above said current frequency.

Claim 42. (New) The method of Claim 40, wherein said c) further comprises increasing voltage at which said computer processor operates prior to said increasing frequency at which said computer processor operates.

Claim 43. (New) The method of Claim 40, wherein:

said b) further comprises determining that said computer processor can be operated at a higher voltage than a current voltage at which said computer processor is operating without exceeding said operating temperature threshold; and

said c) further comprises increasing voltage at which said computer processor operates above said current voltage.

Claim 44. (New) The method of Claim 43, wherein said c) further comprises increasing voltage at which said computer processor operates prior to increasing frequency at which said computer processor operates.

Claim 45. (New) The method of Claim 40, further comprising receiving a set of processor-intensive commands that are to be executed in said computer processor.

Claim 46. (New) A method of controlling a computer processor, comprising:

a) monitoring operating temperature of said computer processor;

b) based on said operating temperature, determining that a voltage at which said computer processor operates can be increased without exceeding a threshold of said operating temperature; and

c) increasing voltage at which said computer processor operates.

Claim 47. (New) The method of Claim 46, wherein said determining further comprises determining a time for which voltage at which said computer processor operates is increased.

Claim 48. (New) A method of managing power consumption comprising:

monitoring internal conditions of a computer processor;

based on said internal conditions, determining an allowable power consumption level;

determining a voltage-frequency pair for said allowable power consumption level; and

dynamically changing power consumption of the computer processor by implementing said voltage-frequency pair.

Claim 49. (New) The method of Claim 48, wherein said dynamically changing power consumption comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 50. (New) The method of Claim 49, wherein said dynamically changing power consumption further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 51. (New) The method of Claim 48, wherein said dynamically changing power consumption comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 52. (New) The method of Claim 48, wherein said implementing comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 53. (New) The method of Claim 49, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 54. (New) The method of Claim 49, wherein said implementing further comprises:

executing instructions in said computer processor after lowering frequency at which said computer processor is operated; and

then lowering voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 55. (New) The method of Claim 49, wherein said implementing further comprises:

lowering voltage at which said computer processor is operated; and

then executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 56. (New) The method of Claim 48, wherein said monitoring comprises monitoring a state of said computer processor.

Claim 57. (New) The method of Claim 56, wherein said state comprises a halt state.

Claim 58. (New) The method of Claim 56, wherein said state comprises a sleep state.

Claim 59. (New) The method of Claim 58, wherein said monitoring further comprises monitoring a halt state of said computer processor.

Claim 60. (New) The method of Claim 48, wherein said monitoring comprises monitoring a temperature.

Claim 61. (New) The method of Claim 60, wherein said monitoring further comprises monitoring a state of said computer processor.

Claim 62. (New) The method of Claim 61, wherein said state comprises a halt state.

Claim 63. (New) The method of Claim 61, wherein said state comprises a sleep state.

Claim 64. (New) The method of Claim 63, wherein said monitoring further comprises monitoring a halt state of said computer processor.

Claim 65. (New) The method of Claim 48, wherein said determining a voltage-frequency pair comprises accessing a table of pre-determined voltage-frequency pairs.

Claim 66. (New) The method of Claim 48, wherein said determining a voltage-frequency pair comprises calculating a voltage-frequency pair.

Claim 67. (New) A method of controlling a computer processor, comprising:

monitoring operating temperature of said computer processor; and

in response to said operating temperature crossing a threshold, dynamically adjusting frequency and voltage at which said computer processor operates to a pre-determined frequency-voltage pair.

Claim 68. (New) The method of Claim 67, wherein said dynamically adjusting comprises accessing a table comprising a plurality of pre-determined frequency-voltage pairs.

Claim 69. (New) The method of Claim 67, wherein said dynamically adjusting comprises increasing voltage at which said computer processor operates prior to increasing frequency at which said computer processor operates.

Claim 70. (New) The method of Claim 69, wherein said dynamically adjusting further comprises lowering frequency at which said computer processor operates prior to lowering voltage at which said computer processor operates.

Claim 71. (New) The method of Claim 67, wherein said dynamically adjusting comprises lowering frequency at which said computer processor operates prior to lowering voltage at which said computer processor operates.

Claim 72. (New) The method of Claim 67, wherein said implementing comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 73. (New) The method of Claim 71, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 74. (New) The method of Claim 71, wherein said implementing further comprises:

executing instructions in said computer processor after lowering frequency at which said computer processor is operated; and

then lowering voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 75. (New) The method of Claim 71, wherein said implementing further comprises:

lowering voltage at which said computer processor is operated; and

then executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 76. (New) A computing device comprising:

a power supply furnishing selectable output voltages;

a clock frequency source; and

a central processor comprising:

a clock frequency generator receiving a clock frequency from the clock frequency source; and

a processing unit operable to provide values indicative of operating conditions of the central processor and to cause the power supply and the clock frequency generator to furnish a voltage level and an output clock frequency for the central processor.

Claim 77. (New) The computing device of Claim 76, wherein:

said clock frequency generator is operable to provide one of a plurality of selectable output clock frequencies to the processing unit.

Claim 78. (New) The computing device of Claim 77, wherein:

said clock frequency generator is further operable to concurrently generate frequencies for a plurality of functional units of the computing device.

Claim 79. (New) The computing device of Claim 76, wherein:

said clock frequency generator is operable to concurrently generate frequencies for a plurality of functional units of the computing device.

Claim 80. (New) The method of Claim 1, wherein said dynamically changing the power consumption comprises increasing voltage prior to increasing frequency.

Claim 81. (New) The method of Claim 60, wherein said dynamically changing the power consumption comprises lowering frequency prior to lowering voltage.

Claim 82. (New) The method of Claim 1, wherein said dynamically changing the power consumption comprises lowering frequency prior to lowering voltage.

Claim 83. (New) The method of Claim 1, wherein said dynamically changing the power consumption comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 84. (New) The method of Claim 82, wherein dynamically changing the power consumption further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 85. (New) The method of Claim 82, wherein dynamically changing the power consumption further comprises:

executing instructions in said computer processor after lowering frequency at which said computer processor is operated; and

then lowering voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 86. (New) The method of Claim 82, wherein dynamically changing the power consumption further comprises:

lowering voltage at which said computer processor is operated; and

then executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 87. (New) The method of Claim 1, wherein said dynamically changing the power consumption comprises concurrently generating a plurality of frequencies.

Claim 88. (New) The method of Claim 1, wherein said operating condition of the processor is internal to the processor.

Claim 89. (New) A method of operating a computer processor comprising an input voltage, an input frequency and an operating temperature, said method comprising:

operating said computer processor with said operating temperature below a pre-selected temperature with said input voltage at a safe voltage level and said input frequency at a safe frequency;

increasing said input voltage to a level higher than said safe voltage level;

increasing said input frequency to a level higher than said safe frequency; and

executing processor-intensive commands while said input voltage is at a level higher than said safe voltage level and said input frequency is at a level higher than said safe frequency.

Claim 90. (New) The method of Claim 89, wherein said executing processor-intensive commands comprises continuing executing said processor-intensive commands until said operating temperature exceeds a pre-determined value.

Claim 91. (New) The method of Claim 89 wherein said executing processor-intensive commands comprises continuing executing said processor-intensive command for no more than a pre-determined time period.

Claim 92. (New) The method of Claim 91, further comprising:

decreasing said input frequency to a level lower than said safe frequency; and

decreasing said input voltage to a level lower than said safe voltage level.